Route design implementation log

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# Vivado v2021.1 (64-bit)

# SW Build 3247384 on Thu Jun 10 19:36:33 MDT 2021

# IP Build 3246043 on Fri Jun 11 00:30:35 MDT 2021

# Start of session at: Wed Apr 10 16:09:35 2024

# Process ID: 3636

# Current directory: E:/project final year/uart\_implementation/uart\_systhesis/uart\_systhesis.runs/impl\_1\_copy\_1

# Command line: vivado.exe -log UART.vdi -applog -product Vivado -messageDb vivado.pb -mode batch -source UART.tcl -notrace

# Log file: E:/project final year/uart\_implementation/uart\_systhesis/uart\_systhesis.runs/impl\_1\_copy\_1/UART.vdi

# Journal file: E:/project final year/uart\_implementation/uart\_systhesis/uart\_systhesis.runs/impl\_1\_copy\_1\vivado.jou

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source UART.tcl -notrace

Command: link\_design -top UART -part xc7z020clg400-1

Design is defaulting to srcset: sources\_1

Design is defaulting to constrset: constrs\_1

INFO: [Device 21-403] Loading part xc7z020clg400-1

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.064 . Memory (MB): peak = 1248.832 ; gain = 0.000

INFO: [Netlist 29-17] Analyzing 3268 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2021.1

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [E:/project final year/UART1systhesis/UART/UART/UART.srcs/constrs\_1/imports/Downloads/Zybo-Z7-Master.xdc]

Finished Parsing XDC File [E:/project final year/UART1systhesis/UART/UART/UART.srcs/constrs\_1/imports/Downloads/Zybo-Z7-Master.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.003 . Memory (MB): peak = 1248.832 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

7 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

link\_design completed successfully

link\_design: Time (s): cpu = 00:00:10 ; elapsed = 00:00:27 . Memory (MB): peak = 1248.832 ; gain = 0.000

Command: opt\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7z020'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z020'

Running DRC as a precondition to command opt\_design

Starting DRC Task

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report\_drc) for more information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.724 . Memory (MB): peak = 1248.832 ; gain = 0.000

Starting Cache Timing Information Task

INFO: [Timing 38-35] Done setting XDC timing constraints.

Ending Cache Timing Information Task | Checksum: d19ddb80

Time (s): cpu = 00:00:06 ; elapsed = 00:00:07 . Memory (MB): peak = 1581.035 ; gain = 332.203

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: d19ddb80

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.535 . Memory (MB): peak = 1795.949 ; gain = 0.168

INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: d19ddb80

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.611 . Memory (MB): peak = 1795.949 ; gain = 0.168

INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: f84abc6f

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.716 . Memory (MB): peak = 1795.949 ; gain = 0.168

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization

Phase 4 BUFG optimization | Checksum: f84abc6f

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.883 . Memory (MB): peak = 1795.949 ; gain = 0.168

INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization

INFO: [Opt 31-1064] SRL Remap converted 0 SRLs to 0 registers and converted 0 registers of register chains to 0 SRLs

Phase 5 Shift Register Optimization | Checksum: f84abc6f

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.902 . Memory (MB): peak = 1795.949 ; gain = 0.168

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist

Phase 6 Post Processing Netlist | Checksum: f84abc6f

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.936 . Memory (MB): peak = 1795.949 ; gain = 0.168

INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Opt\_design Change Summary

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| Phase | #Cells created | #Cells Removed | #Constrained objects preventing optimizations |

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| Retarget | 0 | 0 | 0 |

| Constant propagation | 0 | 0 | 0 |

| Sweep | 0 | 0 | 0 |

| BUFG optimization | 0 | 0 | 0 |

| Shift Register Optimization | 0 | 0 | 0 |

| Post Processing Netlist | 0 | 0 | 0 |

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Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.016 . Memory (MB): peak = 1795.949 ; gain = 0.000

Ending Logic Optimization Task | Checksum: 8b909217

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 1795.949 ; gain = 0.168

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

Ending Power Optimization Task | Checksum: 8b909217

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.014 . Memory (MB): peak = 1795.949 ; gain = 0.000

Starting Final Cleanup Task

Ending Final Cleanup Task | Checksum: 8b909217

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1795.949 ; gain = 0.000

Starting Netlist Obfuscation Task

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.003 . Memory (MB): peak = 1795.949 ; gain = 0.000

Ending Netlist Obfuscation Task | Checksum: 8b909217

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.003 . Memory (MB): peak = 1795.949 ; gain = 0.000

INFO: [Common 17-83] Releasing license: Implementation

24 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

opt\_design completed successfully

opt\_design: Time (s): cpu = 00:00:10 ; elapsed = 00:00:10 . Memory (MB): peak = 1795.949 ; gain = 547.117

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.032 . Memory (MB): peak = 1795.949 ; gain = 0.000

INFO: [Common 17-1381] The checkpoint 'E:/project final year/uart\_implementation/uart\_systhesis/uart\_systhesis.runs/impl\_1\_copy\_1/UART\_opt.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file UART\_drc\_opted.rpt -pb UART\_drc\_opted.pb -rpx UART\_drc\_opted.rpx

Command: report\_drc -file UART\_drc\_opted.rpt -pb UART\_drc\_opted.pb -rpx UART\_drc\_opted.rpx

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2021.1/data/ip'.

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Vivado\_Tcl 2-168] The results of DRC are in file E:/project final year/uart\_implementation/uart\_systhesis/uart\_systhesis.runs/impl\_1\_copy\_1/UART\_drc\_opted.rpt.

report\_drc completed successfully

Command: place\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7z020'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z020'

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Running DRC as a precondition to command place\_design

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place\_design using a maximum of 2 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.004 . Memory (MB): peak = 1859.488 ; gain = 0.000

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 21a917cd

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.009 . Memory (MB): peak = 1859.488 ; gain = 0.000

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.002 . Memory (MB): peak = 1859.488 ; gain = 0.000

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: e044954d

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.693 . Memory (MB): peak = 1859.488 ; gain = 0.000

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: 12006a1b3

Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 1872.520 ; gain = 13.031

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: 12006a1b3

Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 1872.520 ; gain = 13.031

Phase 1 Placer Initialization | Checksum: 12006a1b3

Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 1872.520 ; gain = 13.031

Phase 2 Global Placement

Phase 2.1 Floorplanning

Phase 2.1 Floorplanning | Checksum: fafaf298

Time (s): cpu = 00:00:04 ; elapsed = 00:00:03 . Memory (MB): peak = 1872.520 ; gain = 13.031

Phase 2.2 Update Timing before SLR Path Opt

Phase 2.2 Update Timing before SLR Path Opt | Checksum: 1de039bf8

Time (s): cpu = 00:00:04 ; elapsed = 00:00:04 . Memory (MB): peak = 1872.520 ; gain = 13.031

Phase 2.3 Post-Processing in Floorplanning

Phase 2.3 Post-Processing in Floorplanning | Checksum: 1de039bf8

Time (s): cpu = 00:00:04 ; elapsed = 00:00:04 . Memory (MB): peak = 1872.520 ; gain = 13.031

Phase 2.4 Global Placement Core

Phase 2.4.1 Physical Synthesis In Placer

INFO: [Physopt 32-1035] Found 0 LUTNM shape to break, 828 LUT instances to create LUTNM shape

INFO: [Physopt 32-1044] Break lutnm for timing: one critical 0, two critical 0, total 0, new lutff created 0

INFO: [Physopt 32-1138] End 1 Pass. Optimized 383 nets or LUTs. Breaked 0 LUT, combined 383 existing LUTs and moved 0 existing LUT

INFO: [Physopt 32-65] No nets found for high-fanout optimization.

INFO: [Physopt 32-232] Optimized 0 net. Created 0 new instance.

INFO: [Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell

INFO: [Physopt 32-670] No setup violation found. DSP Register Optimization was not performed.

INFO: [Physopt 32-670] No setup violation found. Shift Register to Pipeline Optimization was not performed.

INFO: [Physopt 32-670] No setup violation found. Shift Register Optimization was not performed.

INFO: [Physopt 32-670] No setup violation found. BRAM Register Optimization was not performed.

INFO: [Physopt 32-670] No setup violation found. URAM Register Optimization was not performed.

INFO: [Physopt 32-949] No candidate nets found for dynamic/static region interface net replication

INFO: [Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.003 . Memory (MB): peak = 1872.520 ; gain = 0.000

Summary of Physical Synthesis Optimizations

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| Optimization | Added Cells | Removed Cells | Optimized Cells/Nets | Dont Touch | Iterations | Elapsed |

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| LUT Combining | 0 | 383 | 383 | 0 | 1 | 00:00:00 |

| Retime | 0 | 0 | 0 | 0 | 1 | 00:00:00 |

| Very High Fanout | 0 | 0 | 0 | 0 | 1 | 00:00:00 |

| DSP Register | 0 | 0 | 0 | 0 | 0 | 00:00:00 |

| Shift Register to Pipeline | 0 | 0 | 0 | 0 | 0 | 00:00:00 |

| Shift Register | 0 | 0 | 0 | 0 | 0 | 00:00:00 |

| BRAM Register | 0 | 0 | 0 | 0 | 0 | 00:00:00 |

| URAM Register | 0 | 0 | 0 | 0 | 0 | 00:00:00 |

| Dynamic/Static Region Interface Net Replication | 0 | 0 | 0 | 0 | 1 | 00:00:00 |

| Total | 0 | 383 | 383 | 0 | 4 | 00:00:00 |

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Phase 2.4.1 Physical Synthesis In Placer | Checksum: 1b097ba83

Time (s): cpu = 00:00:11 ; elapsed = 00:00:09 . Memory (MB): peak = 1872.520 ; gain = 13.031

Phase 2.4 Global Placement Core | Checksum: 1f2a37237

Time (s): cpu = 00:00:12 ; elapsed = 00:00:10 . Memory (MB): peak = 1872.520 ; gain = 13.031

Phase 2 Global Placement | Checksum: 1f2a37237

Time (s): cpu = 00:00:12 ; elapsed = 00:00:10 . Memory (MB): peak = 1872.520 ; gain = 13.031

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: 17c7cdead

Time (s): cpu = 00:00:12 ; elapsed = 00:00:10 . Memory (MB): peak = 1872.520 ; gain = 13.031

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 176b2d449

Time (s): cpu = 00:00:13 ; elapsed = 00:00:11 . Memory (MB): peak = 1872.520 ; gain = 13.031

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: 15463de17

Time (s): cpu = 00:00:13 ; elapsed = 00:00:11 . Memory (MB): peak = 1872.520 ; gain = 13.031

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: 1d4e905a2

Time (s): cpu = 00:00:13 ; elapsed = 00:00:11 . Memory (MB): peak = 1872.520 ; gain = 13.031

Phase 3.5 Fast Optimization

Phase 3.5 Fast Optimization | Checksum: 13cabf4a5

Time (s): cpu = 00:00:14 ; elapsed = 00:00:13 . Memory (MB): peak = 1872.520 ; gain = 13.031

Phase 3.6 Small Shape Detail Placement

Phase 3.6 Small Shape Detail Placement | Checksum: 190c4b4c1

Time (s): cpu = 00:00:18 ; elapsed = 00:00:20 . Memory (MB): peak = 1872.520 ; gain = 13.031

Phase 3.7 Re-assign LUT pins

Phase 3.7 Re-assign LUT pins | Checksum: 13b6f7dec

Time (s): cpu = 00:00:19 ; elapsed = 00:00:21 . Memory (MB): peak = 1872.520 ; gain = 13.031

Phase 3.8 Pipeline Register Optimization

Phase 3.8 Pipeline Register Optimization | Checksum: 1507a329b

Time (s): cpu = 00:00:19 ; elapsed = 00:00:21 . Memory (MB): peak = 1872.520 ; gain = 13.031

Phase 3 Detail Placement | Checksum: 1507a329b

Time (s): cpu = 00:00:19 ; elapsed = 00:00:21 . Memory (MB): peak = 1872.520 ; gain = 13.031

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

INFO: [Timing 38-35] Done setting XDC timing constraints.

Phase 4.1.1 Post Placement Optimization

Post Placement Optimization Initialization | Checksum: 1303de6b8

Phase 4.1.1.1 BUFG Insertion

Starting Physical Synthesis Task

Phase 1 Physical Synthesis Initialization

INFO: [Physopt 32-721] Multithreading enabled for phys\_opt\_design using a maximum of 2 CPUs

INFO: [Physopt 32-619] Estimated Timing Summary | WNS=1.037 | TNS=0.000 |

Phase 1 Physical Synthesis Initialization | Checksum: 15810cf66

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.526 . Memory (MB): peak = 1922.117 ; gain = 0.000

INFO: [Place 46-56] BUFG insertion identified 0 candidate nets. Inserted BUFG: 0, Replicated BUFG Driver: 0, Skipped due to Placement/Routing Conflicts: 0, Skipped due to Timing Degradation: 0, Skipped due to Illegal Netlist: 0.

Ending Physical Synthesis Task | Checksum: 1972a1da3

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.636 . Memory (MB): peak = 1922.117 ; gain = 0.000

Phase 4.1.1.1 BUFG Insertion | Checksum: 1303de6b8

Time (s): cpu = 00:00:21 ; elapsed = 00:00:24 . Memory (MB): peak = 1922.117 ; gain = 62.629

Phase 4.1.1.2 Post Placement Timing Optimization

INFO: [Place 30-746] Post Placement Timing Summary WNS=1.037. For the most accurate timing information please run report\_timing.

Phase 4.1.1.2 Post Placement Timing Optimization | Checksum: 153281426

Time (s): cpu = 00:00:21 ; elapsed = 00:00:24 . Memory (MB): peak = 1922.117 ; gain = 62.629

Time (s): cpu = 00:00:21 ; elapsed = 00:00:24 . Memory (MB): peak = 1922.117 ; gain = 62.629

Phase 4.1 Post Commit Optimization | Checksum: 153281426

Time (s): cpu = 00:00:22 ; elapsed = 00:00:24 . Memory (MB): peak = 1922.117 ; gain = 62.629

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: 153281426

Time (s): cpu = 00:00:22 ; elapsed = 00:00:24 . Memory (MB): peak = 1922.117 ; gain = 62.629

Phase 4.3 Placer Reporting

Phase 4.3.1 Print Estimated Congestion

INFO: [Place 30-612] Post-Placement Estimated Congestion

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| | Global Congestion | Short Congestion |

| Direction | Region Size | Region Size |

|\_\_\_\_\_\_\_\_\_\_\_|\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_|\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_|

| North| 1x1| 2x2|

|\_\_\_\_\_\_\_\_\_\_\_|\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_|\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_|

| South| 1x1| 2x2|

|\_\_\_\_\_\_\_\_\_\_\_|\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_|\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_|

| East| 1x1| 1x1|

|\_\_\_\_\_\_\_\_\_\_\_|\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_|\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_|

| West| 1x1| 1x1|

|\_\_\_\_\_\_\_\_\_\_\_|\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_|\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_|

Phase 4.3.1 Print Estimated Congestion | Checksum: 153281426

Time (s): cpu = 00:00:22 ; elapsed = 00:00:24 . Memory (MB): peak = 1922.117 ; gain = 62.629

Phase 4.3 Placer Reporting | Checksum: 153281426

Time (s): cpu = 00:00:22 ; elapsed = 00:00:24 . Memory (MB): peak = 1922.117 ; gain = 62.629

Phase 4.4 Final Placement Cleanup

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.003 . Memory (MB): peak = 1922.117 ; gain = 0.000

Time (s): cpu = 00:00:22 ; elapsed = 00:00:24 . Memory (MB): peak = 1922.117 ; gain = 62.629

Phase 4 Post Placement Optimization and Clean-Up | Checksum: 110c360c2

Time (s): cpu = 00:00:22 ; elapsed = 00:00:25 . Memory (MB): peak = 1922.117 ; gain = 62.629

Ending Placer Task | Checksum: eaddeff5

Time (s): cpu = 00:00:22 ; elapsed = 00:00:25 . Memory (MB): peak = 1922.117 ; gain = 62.629

INFO: [Common 17-83] Releasing license: Implementation

61 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

place\_design completed successfully

place\_design: Time (s): cpu = 00:00:23 ; elapsed = 00:00:25 . Memory (MB): peak = 1922.117 ; gain = 80.059

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 1922.117 ; gain = 0.000

INFO: [Common 17-1381] The checkpoint 'E:/project final year/uart\_implementation/uart\_systhesis/uart\_systhesis.runs/impl\_1\_copy\_1/UART\_placed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_io -file UART\_io\_placed.rpt

report\_io: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.029 . Memory (MB): peak = 1922.117 ; gain = 0.000

INFO: [runtcl-4] Executing : report\_utilization -file UART\_utilization\_placed.rpt -pb UART\_utilization\_placed.pb

INFO: [runtcl-4] Executing : report\_control\_sets -verbose -file UART\_control\_sets\_placed.rpt

report\_control\_sets: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.072 . Memory (MB): peak = 1922.117 ; gain = 0.000

Command: phys\_opt\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7z020'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z020'

INFO: [Vivado\_Tcl 4-383] Design worst setup slack (WNS) is greater than or equal to 0.000 ns. Skipping all physical synthesis optimizations.

INFO: [Vivado\_Tcl 4-232] No setup violation found. The netlist was not modified.

INFO: [Common 17-83] Releasing license: Implementation

70 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

phys\_opt\_design completed successfully

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:03 ; elapsed = 00:00:01 . Memory (MB): peak = 1949.770 ; gain = 16.801

INFO: [Common 17-1381] The checkpoint 'E:/project final year/uart\_implementation/uart\_systhesis/uart\_systhesis.runs/impl\_1\_copy\_1/UART\_physopt.dcp' has been generated.

Command: route\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7z020'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z020'

Running DRC as a precondition to command route\_design

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route\_design using a maximum of 2 CPUs

Checksum: PlaceDB: 4214919c ConstDB: 0 ShapeSum: a8c95e59 RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: d39af221

Time (s): cpu = 00:00:16 ; elapsed = 00:00:15 . Memory (MB): peak = 2046.219 ; gain = 83.891

Post Restoration Checksum: NetGraph: 25a57dd2 NumContArr: adf5744f Constraints: 0 Timing: 0

Phase 2 Router Initialization

Phase 2.1 Create Timer

Phase 2.1 Create Timer | Checksum: d39af221

Time (s): cpu = 00:00:17 ; elapsed = 00:00:15 . Memory (MB): peak = 2046.219 ; gain = 83.891

Phase 2.2 Fix Topology Constraints

Phase 2.2 Fix Topology Constraints | Checksum: d39af221

Time (s): cpu = 00:00:17 ; elapsed = 00:00:15 . Memory (MB): peak = 2052.805 ; gain = 90.477

Phase 2.3 Pre Route Cleanup

Phase 2.3 Pre Route Cleanup | Checksum: d39af221

Time (s): cpu = 00:00:17 ; elapsed = 00:00:15 . Memory (MB): peak = 2052.805 ; gain = 90.477

Number of Nodes with overlaps = 0

Phase 2.4 Update Timing

Phase 2.4 Update Timing | Checksum: 1b0bace29

Time (s): cpu = 00:00:20 ; elapsed = 00:00:18 . Memory (MB): peak = 2077.574 ; gain = 115.246

INFO: [Route 35-416] Intermediate Timing Summary | WNS=1.306 | TNS=0.000 | WHS=-0.120 | THS=-21.870|

Phase 2 Router Initialization | Checksum: 167edb373

Time (s): cpu = 00:00:22 ; elapsed = 00:00:20 . Memory (MB): peak = 2095.688 ; gain = 133.359

Router Utilization Summary

Global Vertical Routing Utilization = 0 %

Global Horizontal Routing Utilization = 0 %

Routable Net Status\*

\*Does not include unroutable nets such as driverless and loadless.

Run report\_route\_status for detailed report.

Number of Failed Nets = 20195

(Failed Nets is the sum of unrouted and partially routed nets)

Number of Unrouted Nets = 20195

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Phase 3 Initial Routing

Phase 3.1 Global Routing

Phase 3.1 Global Routing | Checksum: 167edb373

Time (s): cpu = 00:00:22 ; elapsed = 00:00:20 . Memory (MB): peak = 2098.043 ; gain = 135.715

Phase 3 Initial Routing | Checksum: 14c287a2f

Time (s): cpu = 00:00:25 ; elapsed = 00:00:22 . Memory (MB): peak = 2125.148 ; gain = 162.820

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 3662

Number of Nodes with overlaps = 270

Number of Nodes with overlaps = 49

Number of Nodes with overlaps = 7

Number of Nodes with overlaps = 1

Number of Nodes with overlaps = 0

INFO: [Route 35-416] Intermediate Timing Summary | WNS=0.781 | TNS=0.000 | WHS=N/A | THS=N/A |

Phase 4.1 Global Iteration 0 | Checksum: 237b4bc9e

Time (s): cpu = 00:00:35 ; elapsed = 00:00:34 . Memory (MB): peak = 2125.148 ; gain = 162.820

Phase 4 Rip-up And Reroute | Checksum: 237b4bc9e

Time (s): cpu = 00:00:35 ; elapsed = 00:00:35 . Memory (MB): peak = 2125.148 ; gain = 162.820

Phase 5 Delay and Skew Optimization

Phase 5.1 Delay CleanUp

Phase 5.1.1 Update Timing

Phase 5.1.1 Update Timing | Checksum: 202bce1eb

Time (s): cpu = 00:00:35 ; elapsed = 00:00:35 . Memory (MB): peak = 2125.148 ; gain = 162.820

INFO: [Route 35-416] Intermediate Timing Summary | WNS=0.887 | TNS=0.000 | WHS=N/A | THS=N/A |

Phase 5.1 Delay CleanUp | Checksum: 202bce1eb

Time (s): cpu = 00:00:35 ; elapsed = 00:00:35 . Memory (MB): peak = 2125.148 ; gain = 162.820

Phase 5.2 Clock Skew Optimization

Phase 5.2 Clock Skew Optimization | Checksum: 202bce1eb

Time (s): cpu = 00:00:35 ; elapsed = 00:00:35 . Memory (MB): peak = 2125.148 ; gain = 162.820

Phase 5 Delay and Skew Optimization | Checksum: 202bce1eb

Time (s): cpu = 00:00:35 ; elapsed = 00:00:35 . Memory (MB): peak = 2125.148 ; gain = 162.820

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1.1 Update Timing

Phase 6.1.1 Update Timing | Checksum: 1f10e081e

Time (s): cpu = 00:00:36 ; elapsed = 00:00:36 . Memory (MB): peak = 2125.148 ; gain = 162.820

INFO: [Route 35-416] Intermediate Timing Summary | WNS=0.887 | TNS=0.000 | WHS=0.058 | THS=0.000 |

Phase 6.1 Hold Fix Iter | Checksum: 20d31cfd4

Time (s): cpu = 00:00:36 ; elapsed = 00:00:36 . Memory (MB): peak = 2125.148 ; gain = 162.820

Phase 6 Post Hold Fix | Checksum: 20d31cfd4

Time (s): cpu = 00:00:36 ; elapsed = 00:00:36 . Memory (MB): peak = 2125.148 ; gain = 162.820

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 5.34327 %

Global Horizontal Routing Utilization = 6.71932 %

Routable Net Status\*

\*Does not include unroutable nets such as driverless and loadless.

Run report\_route\_status for detailed report.

Number of Failed Nets = 0

(Failed Nets is the sum of unrouted and partially routed nets)

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Phase 7 Route finalize | Checksum: 26d98c9b7

Time (s): cpu = 00:00:36 ; elapsed = 00:00:36 . Memory (MB): peak = 2125.148 ; gain = 162.820

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: 26d98c9b7

Time (s): cpu = 00:00:36 ; elapsed = 00:00:36 . Memory (MB): peak = 2125.148 ; gain = 162.820

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: 1a7b508d7

Time (s): cpu = 00:00:37 ; elapsed = 00:00:38 . Memory (MB): peak = 2125.148 ; gain = 162.820

Phase 10 Post Router Timing

INFO: [Route 35-57] Estimated Timing Summary | WNS=0.887 | TNS=0.000 | WHS=0.058 | THS=0.000 |

INFO: [Route 35-327] The final timing numbers are based on the router estimated timing analysis. For a complete and accurate timing signoff, please run report\_timing\_summary.

Phase 10 Post Router Timing | Checksum: 1a7b508d7

Time (s): cpu = 00:00:38 ; elapsed = 00:00:39 . Memory (MB): peak = 2125.148 ; gain = 162.820

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:38 ; elapsed = 00:00:39 . Memory (MB): peak = 2125.148 ; gain = 162.820

Routing Is Done.

INFO: [Common 17-83] Releasing license: Implementation

85 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

route\_design completed successfully

route\_design: Time (s): cpu = 00:00:43 ; elapsed = 00:01:06 . Memory (MB): peak = 2125.148 ; gain = 175.379

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2125.148 ; gain = 0.000

INFO: [Common 17-1381] The checkpoint 'E:/project final year/uart\_implementation/uart\_systhesis/uart\_systhesis.runs/impl\_1\_copy\_1/UART\_routed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file UART\_drc\_routed.rpt -pb UART\_drc\_routed.pb -rpx UART\_drc\_routed.rpx

Command: report\_drc -file UART\_drc\_routed.rpt -pb UART\_drc\_routed.pb -rpx UART\_drc\_routed.rpx

INFO: [IP\_Flow 19-1839] IP Catalog is up to date.

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Vivado\_Tcl 2-168] The results of DRC are in file E:/project final year/uart\_implementation/uart\_systhesis/uart\_systhesis.runs/impl\_1\_copy\_1/UART\_drc\_routed.rpt.

report\_drc completed successfully

INFO: [runtcl-4] Executing : report\_methodology -file UART\_methodology\_drc\_routed.rpt -pb UART\_methodology\_drc\_routed.pb -rpx UART\_methodology\_drc\_routed.rpx

Command: report\_methodology -file UART\_methodology\_drc\_routed.rpt -pb UART\_methodology\_drc\_routed.pb -rpx UART\_methodology\_drc\_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-133] Running Methodology with 2 threads

INFO: [Vivado\_Tcl 2-1520] The results of Report Methodology are in file E:/project final year/uart\_implementation/uart\_systhesis/uart\_systhesis.runs/impl\_1\_copy\_1/UART\_methodology\_drc\_routed.rpt.

report\_methodology completed successfully

INFO: [runtcl-4] Executing : report\_power -file UART\_power\_routed.rpt -pb UART\_power\_summary\_routed.pb -rpx UART\_power\_routed.rpx

Command: report\_power -file UART\_power\_routed.rpt -pb UART\_power\_summary\_routed.pb -rpx UART\_power\_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

97 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

report\_power completed successfully

INFO: [runtcl-4] Executing : report\_route\_status -file UART\_route\_status.rpt -pb UART\_route\_status.pb

INFO: [runtcl-4] Executing : report\_timing\_summary -max\_paths 10 -file UART\_timing\_summary\_routed.rpt -pb UART\_timing\_summary\_routed.pb -rpx UART\_timing\_summary\_routed.rpx -warn\_on\_violation

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

INFO: [runtcl-4] Executing : report\_incremental\_reuse -file UART\_incremental\_reuse\_routed.rpt

INFO: [Vivado\_Tcl 4-1062] Incremental flow is disabled. No incremental reuse Info to report.

INFO: [runtcl-4] Executing : report\_clock\_utilization -file UART\_clock\_utilization\_routed.rpt

INFO: [runtcl-4] Executing : report\_bus\_skew -warn\_on\_violation -file UART\_bus\_skew\_routed.rpt -pb UART\_bus\_skew\_routed.pb -rpx UART\_bus\_skew\_routed.rpx

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

INFO: [Common 17-206] Exiting Vivado at Wed Apr 10 16:12:18 2024...

#-----------------------------------------------------------

# Vivado v2021.1 (64-bit)

# SW Build 3247384 on Thu Jun 10 19:36:33 MDT 2021

# IP Build 3246043 on Fri Jun 11 00:30:35 MDT 2021

# Start of session at: Wed Apr 10 16:29:38 2024

# Process ID: 10912

# Current directory: E:/project final year/uart\_implementation/uart\_systhesis/uart\_systhesis.runs/impl\_1\_copy\_1

# Command line: vivado.exe -log UART.vdi -applog -product Vivado -messageDb vivado.pb -mode batch -source UART.tcl -notrace

# Log file: E:/project final year/uart\_implementation/uart\_systhesis/uart\_systhesis.runs/impl\_1\_copy\_1/UART.vdi

# Journal file: E:/project final year/uart\_implementation/uart\_systhesis/uart\_systhesis.runs/impl\_1\_copy\_1\vivado.jou

#-----------------------------------------------------------

source UART.tcl -notrace

Command: open\_checkpoint UART\_routed.dcp

Starting open\_checkpoint Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.091 . Memory (MB): peak = 1211.023 ; gain = 0.000

INFO: [Device 21-403] Loading part xc7z020clg400-1

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.064 . Memory (MB): peak = 1211.023 ; gain = 0.000

INFO: [Netlist 29-17] Analyzing 3268 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2021.1

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Timing 38-478] Restoring timing data from binary archive.

INFO: [Timing 38-479] Binary timing data restore complete.

INFO: [Project 1-856] Restoring constraints from binary archive.

INFO: [Project 1-853] Binary constraint restore complete.

Reading XDEF placement.

Reading placer database...

Reading XDEF routing.

Read XDEF File: Time (s): cpu = 00:00:02 ; elapsed = 00:00:01 . Memory (MB): peak = 1591.836 ; gain = 9.977

Restored from archive | CPU: 2.000000 secs | Memory: 0.000000 MB |

Finished XDEF File Restore: Time (s): cpu = 00:00:02 ; elapsed = 00:00:01 . Memory (MB): peak = 1591.836 ; gain = 9.977

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.004 . Memory (MB): peak = 1591.836 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2021.1 (64-bit) build 3247384

open\_checkpoint: Time (s): cpu = 00:00:13 ; elapsed = 00:00:39 . Memory (MB): peak = 1594.105 ; gain = 383.082

Command: write\_bitstream -force UART.bit

Attempting to get a license for feature 'Implementation' and/or device 'xc7z020'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z020'

Running DRC as a precondition to command write\_bitstream

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2021.1/data/ip'.

INFO: [DRC 23-27] Running DRC with 2 threads

WARNING: [DRC ZPS7-1] PS7 block required: The PS7 cell must be used in this Zynq design in order to enable correct default configuration.

INFO: [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings

INFO: [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.

INFO: [Designutils 20-2272] Running write\_bitstream with 2 threads.

Loading data files...

Loading site data...

Loading route data...

Processing options...

Creating bitmap...

Creating bitstream...

Writing bitstream ./UART.bit...

INFO: [Vivado 12-1842] Bitgen Completed Successfully.

INFO: [#UNDEF] WebTalk data collection is mandatory when using a WebPACK part without a full Vivado license. To see the specific WebTalk data collected for your design, open the usage\_statistics\_webtalk.html or usage\_statistics\_webtalk.xml file in the implementation directory.

INFO: [Common 17-83] Releasing license: Implementation

22 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

write\_bitstream completed successfully

write\_bitstream: Time (s): cpu = 00:00:24 ; elapsed = 00:00:59 . Memory (MB): peak = 2216.219 ; gain = 622.113

INFO: [Common 17-206] Exiting Vivado at Wed Apr 10 16:31:29 2024...